KVR667D2S8F5/1GHE
1GB 128M x 72-Bit PC2-5300
CL5 ECC 240-Pin FBDIMM

Description:

This document describes ValueRAM's 1GB (128M x 72-bit) PC2-5300 CL5 SDRAM (Synchronous DRAM) "fully buffered" ECC "single rank" memory module. This module is based on nine 128M x 8-bit 667MHz DDR2 FBGA components. The module also includes an AMB device (Advanced Memory Buffer). The electrical and mechanical specifications are as follows:

Feature:

- FBDIMM Module: 240-pin
- JEDEC Standard: R/C A
- Memory Organization: 1 rank of x8 devices
- DDR2 DRAM Interface: SSTL_18
- DDR2 Speed Grade: 667 Mbps
- CAS Latency: 5-5-5
- Module Bandwidth: 5.3 GB/s
- DRAM: VDD = VDDQ = 1.8V
- AMB: VCC = VCCFBD = 1.5V
- EEPROM: VDDSPD = 3.3V (typical)
- Heat Spreader: Full DIMM Heat Spreader (FDHS)
- PCB Height: 30.35mm, double-side
- RoHS Compliant

DRAM Supported:

Hynix E-die

DDR2 240-pin FBDIMM Pinout:

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V_{DD}	121	V_{DD}	31	PN3	151	SN3	61	$\overline{PN9}$	181	$\overline{SN9}$	91	$\overline{PS9}$	211	$\overline{SS9}$
2	V_{DD}	122	V_{DD}	32	$\overline{PN3}$	152	$\overline{SN3}$	62	V_{SS}	182	V_{SS}	92	V_{SS}	212	V_{SS}
3	V_{DD}	123	V_{DD}	33	V_{SS}	153	V_{SS}	63	PN10	183	SN10	93	PS5	213	SS5
4	V_{SS}	124	V_{SS}	34	PN4	154	SN4	64	$\overline{PN10}$	184	$\overline{SN10}$	94	$\overline{PS5}$	214	$\overline{SS5}$
5	V_{DD}	125	V_{DD}	35	$\overline{PN4}$	155	$\overline{SN4}$	65	V_{SS}	185	V_{SS}	95	V_{SS}	215	V_{SS}
6	V_{DD}	126	V_{DD}	36	V_{SS}	156	V_{SS}	66	PN11	186	SN11	96	PS6	216	SS6
7	V_{DD}	127	V_{DD}	37	PN5	157	SN5	67	$\overline{PN11}$	187	$\overline{SN11}$	97	$\overline{PS6}$	217	$\overline{SS6}$
8	V_{SS}	128	V_{SS}	38	$\overline{PN5}$	158	$\overline{SN5}$	68	V_{SS}	188	V_{SS}	98	V_{SS}	218	V_{SS}
9	V_{CC}	129	V_{CC}	39	V_{SS}	159	V_{SS}	KEY				99	PS7	219	SS7
10	V_{CC}	130	V_{CC}	40	PN13	160	SN13	69	V_{SS}	189	V_{SS}	100	$\overline{PS7}$	220	$\overline{SS7}$
11	V_{SS}	131	V_{SS}	41	$\overline{PN13}$	161	$\overline{SN13}$	70	PS0	190	SS0	101	V_{SS}	221	V_{SS}
12	V_{CC}	132	V_{CC}	42	V_{SS}	162	V_{SS}	71	$\overline{PS0}$	191	$\overline{SS0}$	102	PS8	222	SS8
13	V_{CC}	133	V_{CC}	43	V_{SS}	163	V_{SS}	72	V_{SS}	192	V_{SS}	103	$\overline{PS8}$	223	$\overline{SS8}$
14	V_{SS}	134	V_{SS}	44	RFU*	164	RFU*	73	PS1	193	SS1	104	V_{SS}	224	V_{SS}
15	V_{TT}	135	V_{TT}	45	RFU*	165	RFU*	74	$\overline{PS1}$	194	$\overline{SS1}$	105	RFU**	225	RFU**
16	VID1	136	VID0	46	V_{SS}	166	V_{SS}	75	V_{SS}	195	V_{SS}	106	RFU**	226	RFU**
17	$\overline{RESET}$	137	DNU/M_Test	47	V_{SS}	167	V_{SS}	76	PS2	196	SS2	107	V_{SS}	227	V_{SS}
18	V_{SS}	138	V_{SS}	48	PN12	168	SN12	77	$\overline{PS2}$	197	$\overline{SS2}$	108	V_{DD}	228	SCK
19	RFU**	139	RFU**	49	$\overline{PN12}$	169	$\overline{SN12}$	78	V_{SS}	198	V_{SS}	109	V_{DD}	229	$\overline{SCK}$
20	RFU**	140	RFU**	50	V_{SS}	170	V_{SS}	79	PS3	199	SS3	110	V_{SS}	230	V_{SS}
21	V_{SS}	141	V_{SS}	51	PN6	171	SN6	80	$\overline{PS3}$	200	$\overline{SS3}$	111	V_{DD}	231	V_{DD}
22	PN0	142	SN0	52	$\overline{PN6}$	172	$\overline{SN6}$	81	V_{SS}	201	V_{SS}	112	V_{DD}	232	V_{DD}
23	$\overline{PN0}$	143	$\overline{SN0}$	53	V_{SS}	173	V_{SS}	82	PS4	202	SS4	113	V_{DD}	233	V_{DD}
24	V_{SS}	144	V_{SS}	54	PN7	174	SN7	83	$\overline{PS4}$	203	$\overline{SS4}$	114	V_{SS}	234	V_{SS}
25	PN1	145	SN1	55	$\overline{PN7}$	175	$\overline{SN7}$	84	V_{SS}	204	V_{SS}	115	V_{DD}	235	V_{DD}
26	$\overline{PN1}$	146	$\overline{SN1}$	56	V_{SS}	176	V_{SS}	85	V_{SS}	205	V_{SS}	116	V_{DD}	236	V_{DD}
27	V_{SS}	147	V_{SS}	57	PN8	177	SN8	86	RFU*	206	RFU*	117	V_{TT}	237	V_{TT}
28	PN2	148	SN2	58	$\overline{PN8}$	178	$\overline{SN8}$	87	RFU*	207	RFU*	118	SA2	238	VDDSPD
29	$\overline{PN2}$	149	$\overline{SN2}$	59	V_{SS}	179	V_{SS}	88	V_{SS}	208	V_{SS}	119	SDA	239	SA0
30	V_{SS}	150	V_{SS}	60	PN9	180	SN9	89	V_{SS}	209	V_{SS}	120	SCL	240	SA1
								90	PS9	210	SS9				

RFU = Reserved Future Use.
* These pin positions are reserved for forwarded clocks to be used in future module implementations
** These pin positions are reserved for future architecture flexibility
1) The following signals are CRC bits and thus appear out of the normal sequence: PN12/$\overline{PN12}$, SN12/$\overline{SN12}$, PN13/$\overline{PN13}$, SN13/$\overline{SN13}$, PS9/$\overline{PS9}$, SS9/$\overline{SS9}$

DIMM Connector Pin Description:

Pin Name	Pin Description	Count
SCK	System Clock Input, positive line[1]	1
$\overline{SCK}$	System Clock Input, negative line[1]	1
PN[13:0]	Primary Northbound Data, positive lines	14
$\overline{PN}$[13:0]	Primary Northbound Data, negative lines	14
PS[9:0]	Primary Southbound Data, positive lines	10
$\overline{PS}$[9:0]	Primary Southbound Data, negative lines	10
SN[13:0]	Secondary Northbound Data, positive lines	14
$\overline{SN}$[13:0]	Secondary Northbound Data, negative lines	14
SS[9:0]	Secondary Southbound Data, positive lines	10
$\overline{SS}$[9:0]	Secondary Southbound Data, negative lines	10
SCL	Serial Presence Detect (SPD) Clock Input	1
SDA	SPD Data Input / Output	1
SA[2:0]	SPD Address Inputs, also used to select the DIMM number in the AMB	3
VID[1:0]	Voltage ID: These pins must be unconnected for DDR2-based Fully Buffered DIMMs VID[0] is V_{DD} value: OPEN = 1.8 V, GND = 1.5 V; VID[1] is V_{CC} value: OPEN = 1.5 V, GND = 1.2 V	2
$\overline{RESET}$	AMB reset signal	1
RFU	Reserved for Future Use[2]	16
V_{CC}	AMB Core Power and AMB Channel Interface Power (1.5 Volt)	8
V_{DD}	DRAM Power and AMB DRAM I/O Power (1.8 Volt)	24
V_{TT}	DRAM Address/Command/Clock Termination Power (V_{DD}/2)	4
V_{DDSPD}	SPD Power	1
V_{SS}	Ground	80
DNU/M_Test	The DNU/M_Test pin provides an external connection on R/Cs A-D for testing the margin of Vref which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and if it does, will be included in this specification at that time. 1	1
	Total	240

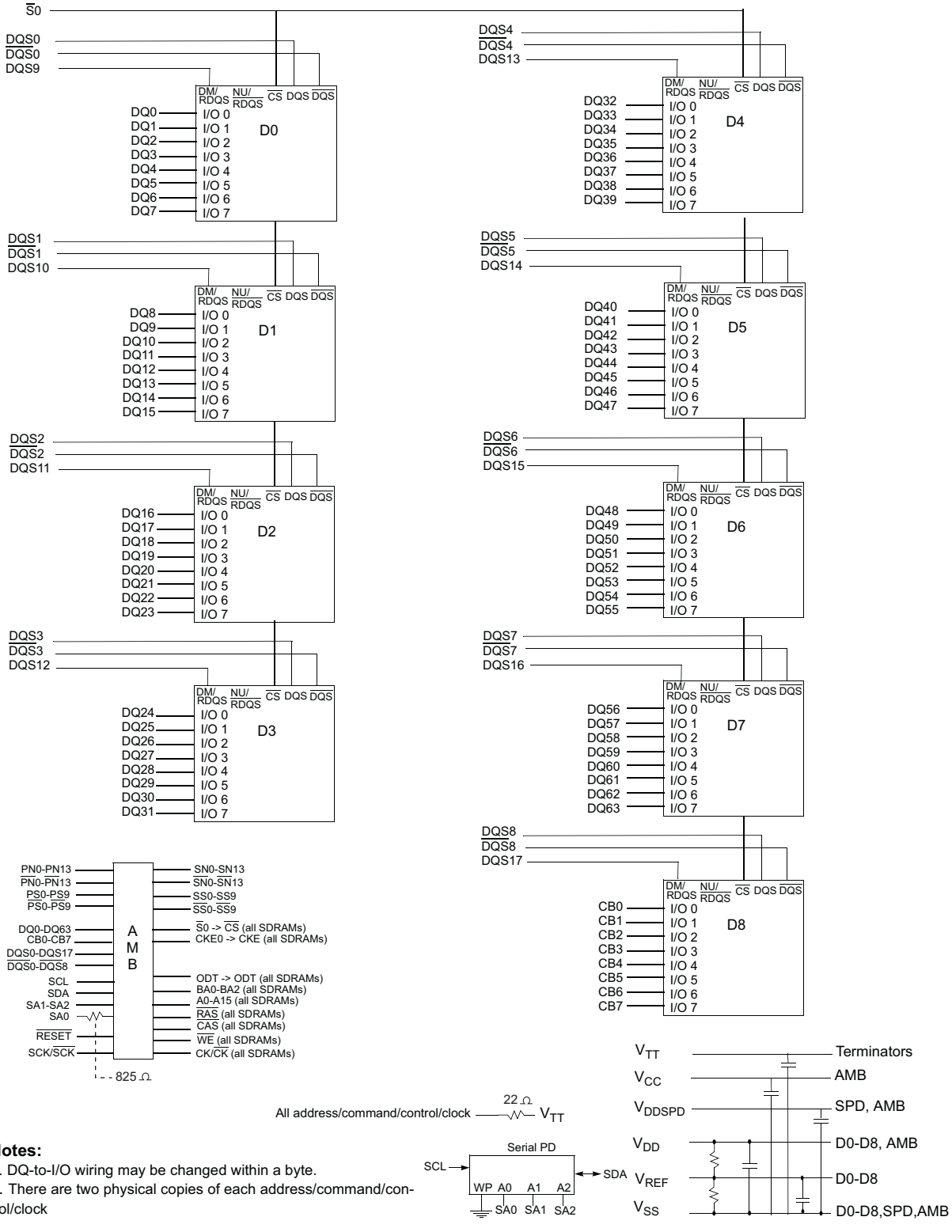
1. System Clock Signals SCK and $\overline{SCK}$ switch at one half the DRAM CK/$\overline{CK}$ frequency
2. Eight pins reserved for forwarded clocks, eight pins reserved for future architecture flexibility

Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Units
VIN, VOUT	Voltage on any pin relative to V_{SS}	-0.3	1.75	V
VCC	Voltage on V_{CC} pin relative to V_{SS}	-0.3	1.75	V
VDD	Voltage V_{DD} pin relative to Vss	-0.5	2.3	V
VTT	Voltage on V_{TT} pin relative to V_{SS}	-0.5	2.3	V
T_{STG}	Storage temperature	-55	100	°C
T_{CASE}	DDR2 SDRAM device operating temperature (Ambient)	0	95 (1)	°C
	AMB device operating temperature (Ambient)	0	110	°C

Note: (1) Above 85°C DRAM case temperature the Auto-Refresh command interval has to be reduced to tREFI = 3.9 µs.

Functional Block Diagram:



Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. There are two physical copies of each address/command/control/clock

Architecture:

Advanced Memory Buffer Pin Description:

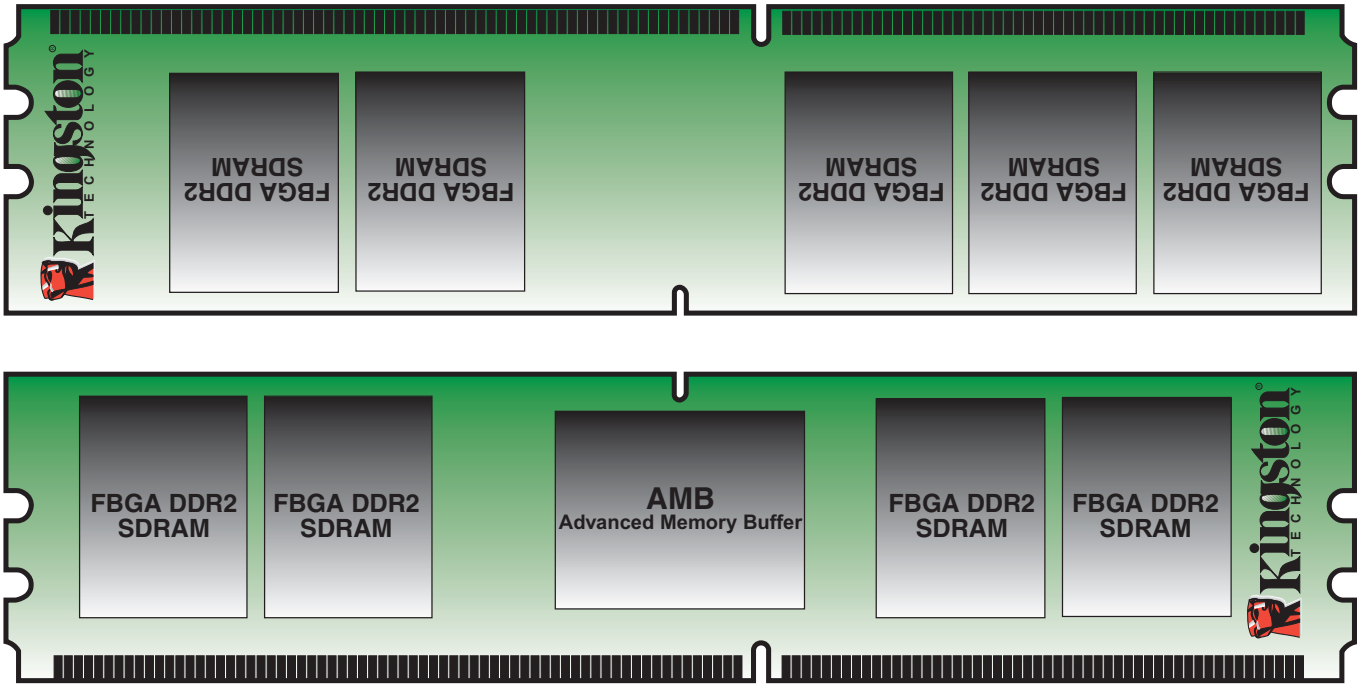
Pin Name	Pin Description	Count
FB-DIMM Channel Signals		**99**
SCK	System Clock Input, positive line	1
$\overline{\text{SCK}}$	System Clock Input, negative line	1
PN[13:0]	Primary Northbound Data, positive lines	14
$\overline{\text{PN}}$[13:0]	Primary Northbound Data, negative lines	14
PS[9:0]	Primary Southbound Data, positive lines	10
$\overline{\text{PS}}$[9:0]	Primary Southbound Data, negative lines	10
SN[13:0]	Secondary Northbound Data, positive lines	14
$\overline{\text{SN}}$[13:0]	Secondary Northbound Data, negative lines	14
SS[9:0]	Secondary Southbound Data, positive lines	10
$\overline{\text{SS}}$[9:0]	Secondary Southbound Data, negative lines	10
FBDRES	To an external precision calibration resistor connected to Vcc	1
DDR2 Interface Signals		**175**
DQS[8:0]	Data Strobes, positive lines	9
$\overline{\text{DQS}}$[8:0]	Data Strobes, negative lines	9
DQS[17:9]/DM[8:0]	Data Strobes (x4 DRAM only), positive lines. These signals are driven low to x8 DRAM on writes.	9
$\overline{\text{DQS}}$[17:9]	Data Strobes (x4 DRAM only), negative lines	9
DQ[63:0]	Data	64
CB[7:0]	Checkbits	8
A[15:0]A, A[15:0]B	Addresses. A10 is part of the pre-charge command	32
BA[2:0]A, BA[2:0]B	Bank Addresses	6
$\overline{\text{RAS}}$A, $\overline{\text{RAS}}$B	Part of command, with $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and $\overline{\text{CS}}$[1:0].	2
$\overline{\text{CAS}}$A, $\overline{\text{CAS}}$B	Part of command, with $\overline{\text{RAS}}$, $\overline{\text{WE}}$, and $\overline{\text{CS}}$[1:0].	2
$\overline{\text{WE}}$A, $\overline{\text{WE}}$B	Part of command, with $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{CS}}$[1:0].	2
ODTA, ODTB	On-die Termination Enable	2
CKE[1:0]A, CKE[1:0]B	Clock Enable (one per rank)	4
$\overline{\text{CS}}$[1:0]A, $\overline{\text{CS}}$[1:0]B	Chip Select (one per rank)	4
CLK[3:0]	CLK[1:0] used on 9 and 18 device DIMMs, CLK[3:0] used on 36 device DIMMs. CLK[3:2] should be output disabled when not in use.	4
$\overline{\text{CLK}}$[3:0]	Negative lines for CLK[3:0]	4
DDRC_C14	DDR Compensation: Common return pin for DDRC_B18 and DDRC_C18.	1
DDRC_B18	DDR Compensation: Resistor connected to common return pin DDRC_C14	1
DDRC_C18	DDR Compensation: Resistor connected to common return pin DDRC_C14	1
DDRC_B12	DDR Compensation: Resistor connected to V_{SS}	1
DDRC_C12	DDR Compensation: Resistor connected to V_{DD}	1

Advanced Memory Buffer Pin Description:

SPD Bus Interface Signals		**5**
SCL	Serial Presence Detect (SPD) Clock Input	1
SDA	SPD Data Input / Output	1
SA[2:0]	SPD Address Inputs, also used to select the DIMM number in the AMB	3
Miscellaneous Signals		**163**
PLLTSTO	PLL Clock Observability Output	1
VCCAPLL	Analog VCC for the PLL. Tied with low pass filter to VCC.	1
VSSAPLL	Analog VSS for the PLL. Tied to ground on the AMB die. Do not tie to ground on the DIMM.	1
TEST_pin#	Leave floating on the DIMM	6
TESTLO_pin#	Tie to ground on the DIMM[2]	5
BFUNC	Tie to ground to set functionality as “buffer on DIMM.”	1
$\overline{\text{RESET}}$	AMB reset signal	1
NC	No connect. Many NC are connected to VDD on the DIMM, to lower the impedance of the VDD power islands.	129
RFU	Reserved for Future Use	18
Power/Ground Signals		**213**
V_{CC}	AMB Core Power (1.5 Volt)	24
V_{CCFBD}	AMB Channel I/O Power (1.5 Volt)	8
V_{DD}	AMB DRAM I/O Power (1.8 Volt)	24
V_{DDSPD}	SPD Power (3.3 Volt)	1
V_{SS}	Ground	156
	Total	**655**

1. System Clock Signals SCK and $\overline{\text{SCK}}$ switch at one half the DRAM CK/$\overline{\text{CK}}$ frequency.
2. TESTLO_AB20 and TESTLO_AC20 should be configured for debug purposes on prototype DIMMs: each pin should have a zero ohm resistor pulldown to ground, and an unpopulated resistor pullup to VCC. These resistors can be replaced on production DIMMs with a direct connection to ground.

Package Dimensions:



(Units = millimeters)